

Linear Memory Schema

FIGURE 1

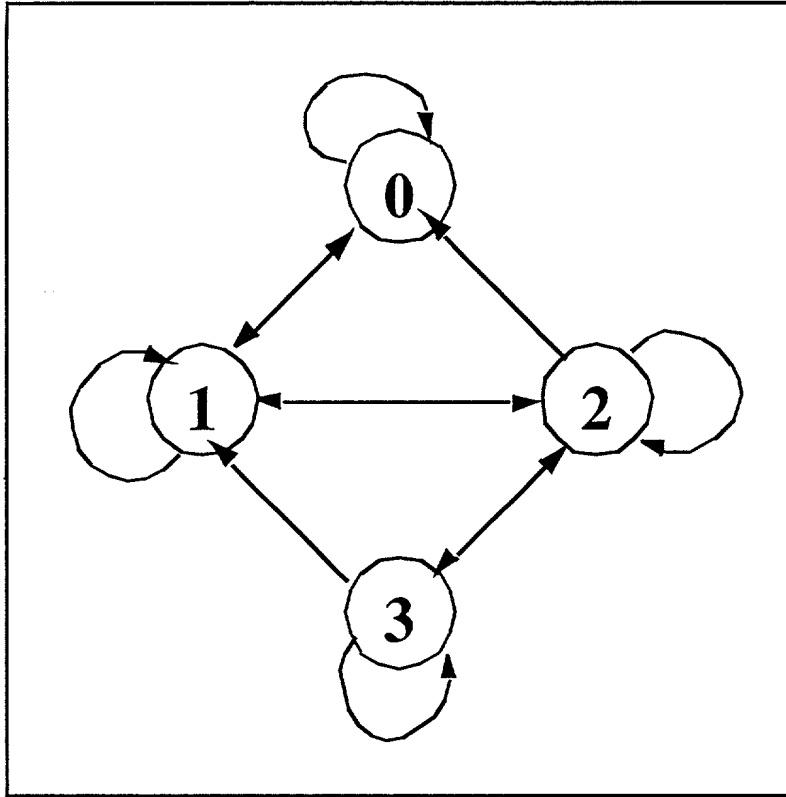


Figure 2 Transitions of State Variable X_i

Invariant:

**$(X_i=3) \Rightarrow$ incoming links have
at most one request**

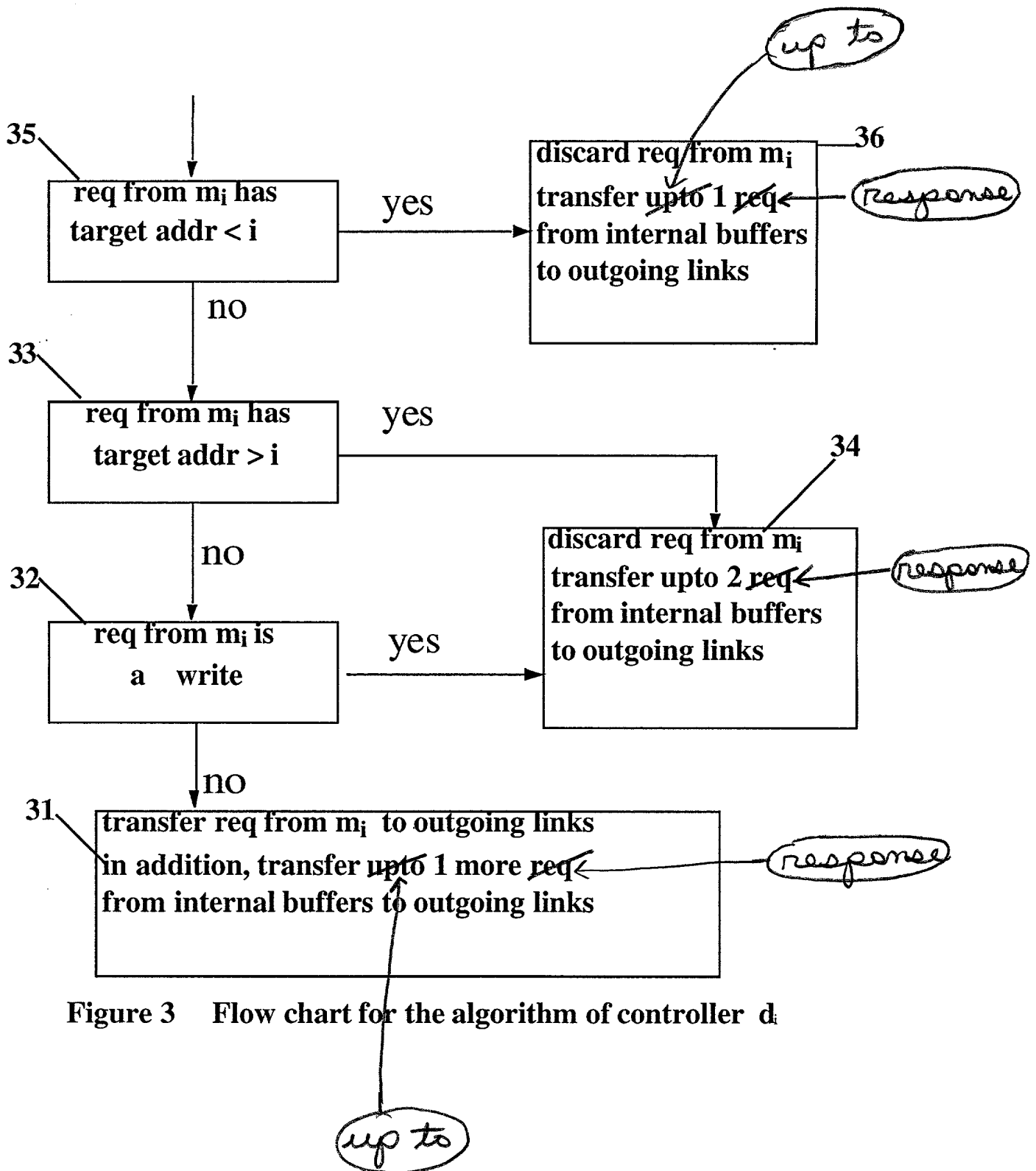


Figure 3 Flow chart for the algorithm of controller d_i

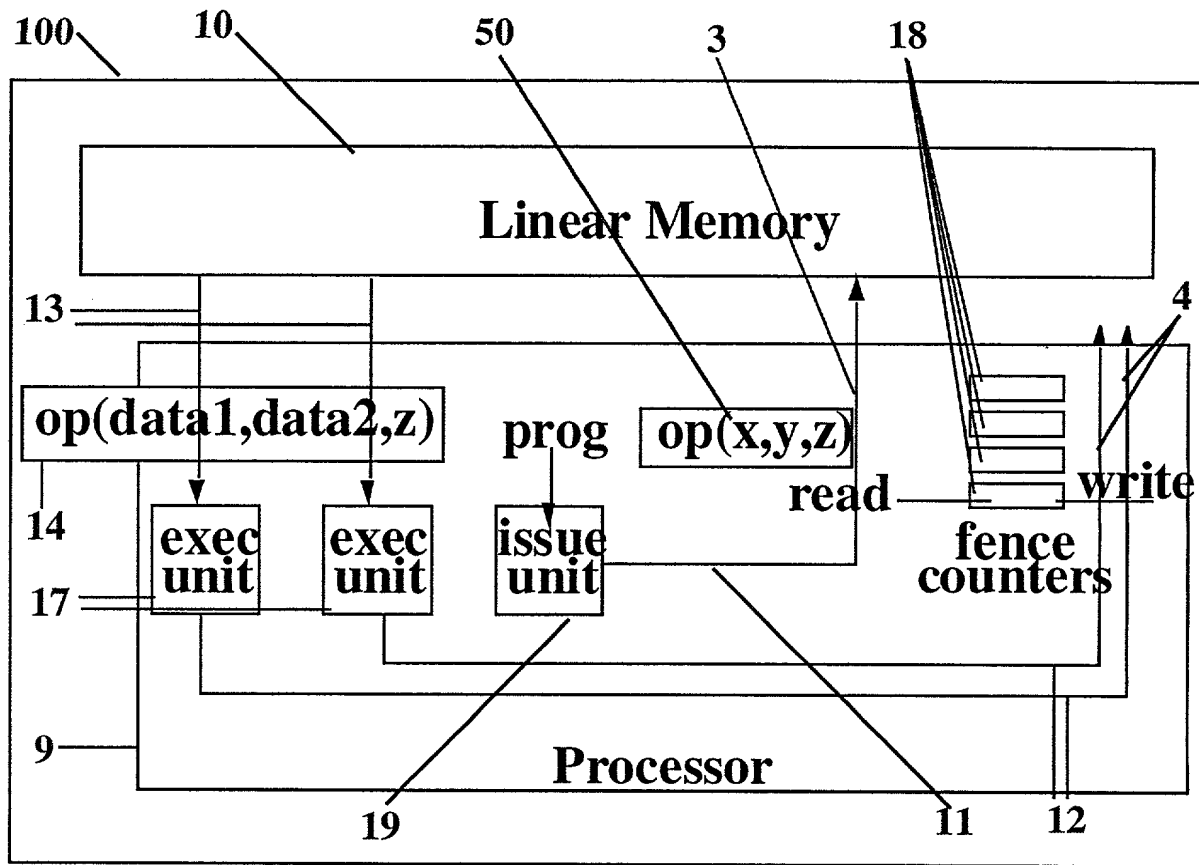


Figure 4 Scalable Processor Schema

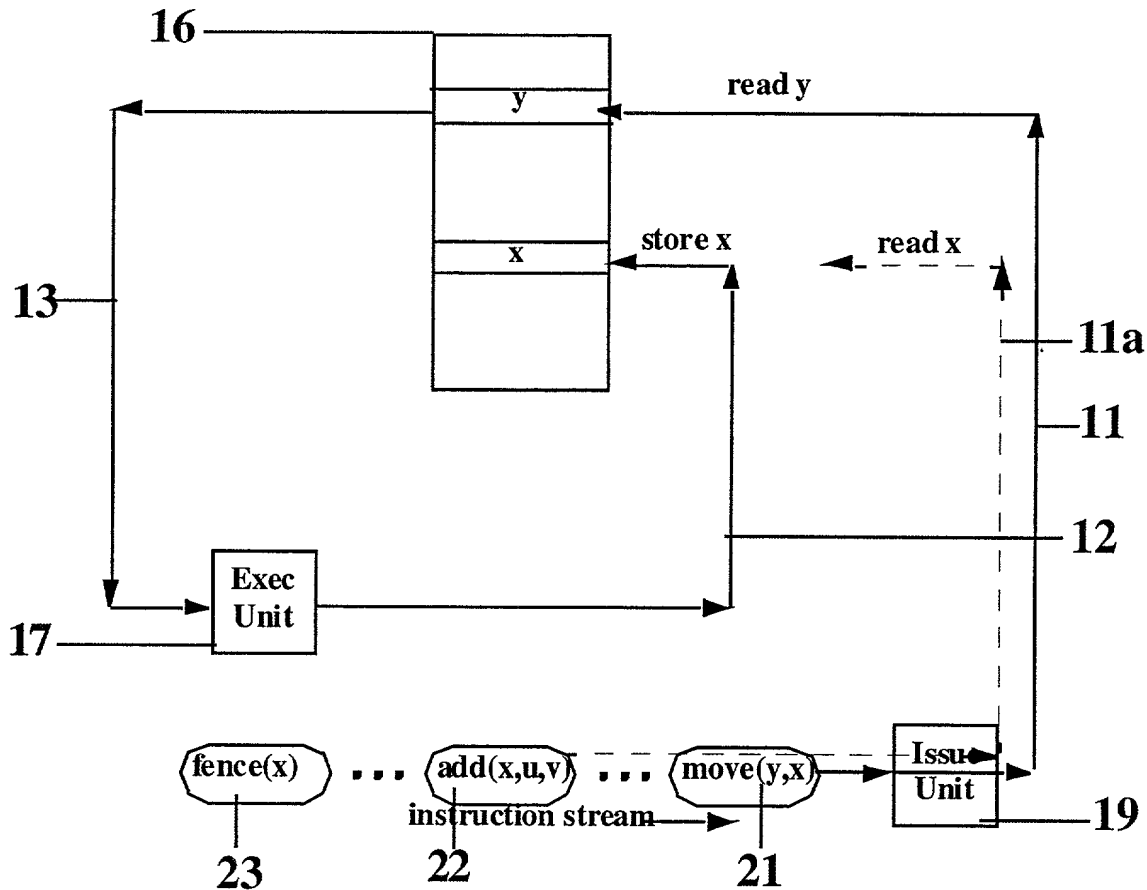
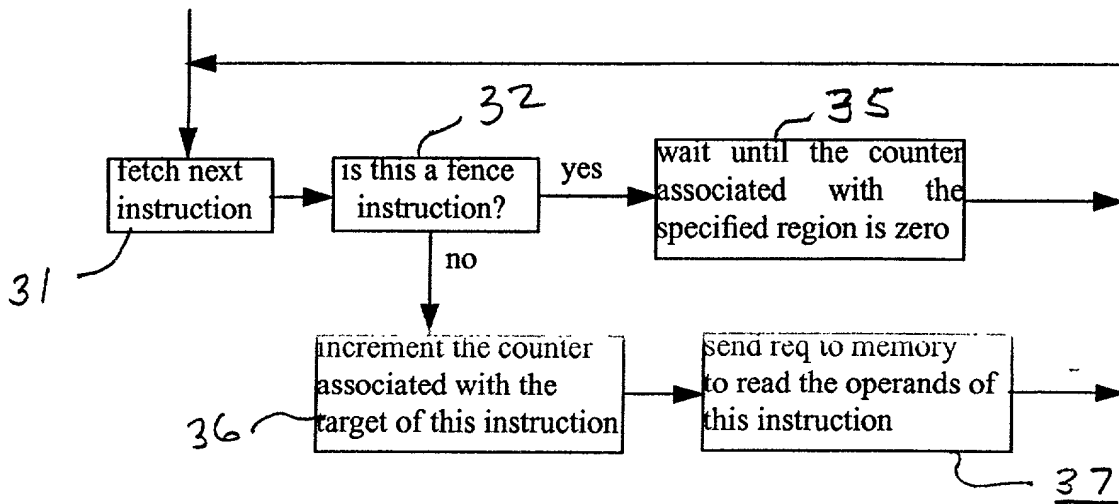


Figure 5 Diagram illustrating read-write-hazard: the path of solid lines illustrates how the move instruction is executed. When it is issued, it goes and reads location *y* and the data flows into the execution unit. When it executes, the result is sent to be stored in location *x*. However, the issue unit proceeds concurrently and issues other instructions following it. The add instruction is an example of a subsequent instruction that uses *x* and its path is illustrated by the dashed line. If this is issued before the previous store to *x* takes place, we have a hazard.



Flow Chart for the algorithm of the Issue Unit

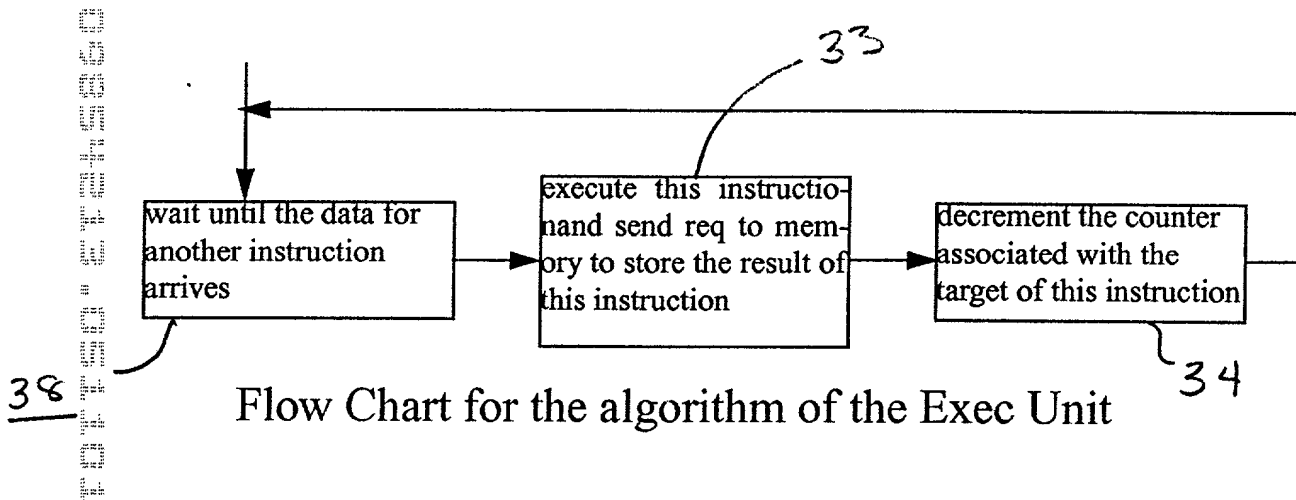


FIGURE 6